# **NTMS4101P**

# **Trench Power MOSFET**

20 V, 9.0 A, Single P-Channel, SO-8

# **Features**

- Leading -20 V Trench for Low R<sub>DS(on)</sub>
- Surface Mount SO-8 Package Saves Board Space
- Lead-Free Package for Green Manufacturing (G Suffix)

# **Applications**

- Power Management
- Load Switch
- Battery Protection

# **MAXIMUM RATINGS** (T<sub>J</sub> = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Drain-to-Source Voltage		V <sub>DSS</sub>	-20	V
Gate-to-Source Voltage		V <sub>GS</sub>	±8.0	V
Continuous Drain Current	Steady State		-6.9	
Continuous Drain Current	t ≤ 10 s	ID	-9.0	Α
Pulsed Drain Current	t = 10 μs	I <sub>DM</sub>	-30	Α
Power Dissipation	Steady State	$P_{D}$	1.38	W
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	ဗို
Continuous Source Current (Body Diode)		I <sub>S</sub>	-6.9	Α
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)		TL	260	°C

# THERMAL RESISTANCE RATINGS

Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	90	°C/W
Junction-to-Ambient - t ≤ 10 s (Note 1)	$R_{ heta JA}$	50	

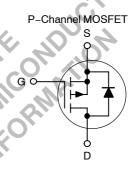
<sup>1.</sup> Surface-mounted on FR4 board using 1" sq. pad size (Cu. area = 1.127 in. sq. [1 oz.] including traces).



# ON Semiconductor®

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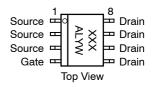
V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX
-20 V	▶ 16 mΩ @ −4.5 V	-9.0 A
20 (	22 mΩ @ -2.5 V	3.071



## **MARKING DIAGRAM & PIN ASSIGNMENT**



SO-8 **CASE 751** STYLE 12



XXX = Specific Device Code = Assembly Location

= Wafer Lot = Year

# = Work Week

Device	Package	Shipping
NTMS4101PR2	SO-8	2500/Reel
NTMS4101PR2G	SO-8 (Pb-Free)	2500/Reel

**ORDERING INFORMATION** 

# NTMS4101P

# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{GS} = 0 \text{ V, } I_D = -250 \mu\text{A}$	V <sub>(BR)DSS</sub>	-20			V
Zero Gate Voltage Drain Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -16 V	I <sub>DSS</sub>			-10	μΑ
Gate-to-Source Leakage Current	V <sub>GS</sub> = ±8.0 V, V <sub>DS</sub> = 0 V	I <sub>GSS</sub>			±100	nA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	V <sub>GS(th)</sub>	-0.45			V
Drain-to-Source On-Resistance	$V_{GS} = -4.5 \text{ V}, I_D = -6.9 \text{ A}$	R <sub>DS(on)</sub>		16	19	mΩ
	$V_{GS} = -2.5 \text{ V}, I_D = -6.5 \text{ A}$			22	30	
Forward Transconductance	$V_{DS} = -15 \text{ V}, I_D = -6.9 \text{ A}$	9FS		70		S
CHARGES AND CAPACITANCES		<b>4 1</b> 7				
Input Capacitance		C <sub>iss</sub>		3200	0	pF
Output Capacitance	$V_{GS} = 0 \text{ V, f} = 1 \text{ MHz,} $ $V_{DS} = -10 \text{ V}$	C <sub>oss</sub>		320		
Reverse Transfer Capacitance		C <sub>rss</sub>		192	)	1
Total Gate Charge		Q <sub>G(TOT)</sub>		29.5	32	nC
Gate-to-Source Charge	$V_{GS} = -4.5 \text{ V}, V_{DS} = -10 \text{ V},$ $I_{D} = -6.9 \text{ A}$	Q <sub>GS</sub>	<b>V</b> 3	6.0	1	
Gate-to-Drain Charge		$Q_{GD}$	.0	7.5		
SWITCHING CHARACTERISTICS (Note	3)		, O.	<b>D</b> ,		
Turn-On Delay Time		t <sub>d(on)</sub>		12.5		ns
Rise Time	$V_{GS} = -4.5 \text{ V}, V_{DD} = -10 \text{ V},$ $I_{D} = -1.0 \text{ A}, R_{G} = 6.0 \Omega$	Ę.	,O,	9.0		1
Turn-Off Delay Time	$I_D = -1.0 \text{ A}, R_G = 6.0 \Omega$	t <sub>d(off)</sub>	X	144		1
Fall Time		t <sub>f</sub>		38.5		
DRAIN-SOURCE DIODE CHARACTER	STICS	0				
Forward Diode Voltage	$V_{GS} = 0 \text{ V, } l_S = -6.9 \text{ A}$	V <sub>SD</sub>		0.72	0.95	V
Reverse Recovery Time	00/4/16	t <sub>rr</sub>		28	35	ns
Charge Time	$V_{GS} = 0 \text{ V}, V_{DS} = -10 \text{ V},$	ta		12		
Discharge Time	$dl_S/dt = 100 \text{ A/}\mu\text{s}, l_S = -6.9 \text{ A}$	t <sub>b</sub>		15		1
Reverse Recovery Charge		Q <sub>rr</sub>		.017		nC

Pulse Test: Pulse Width ≤[300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperature.

# TYPICAL PERFORMANCE CURVES (T<sub>J</sub> = 25°C unless otherwise noted)

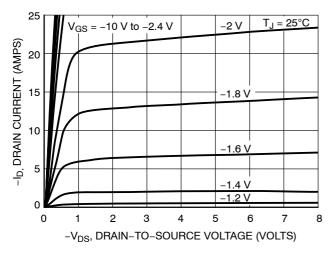


Figure 1. On-Region Characteristics

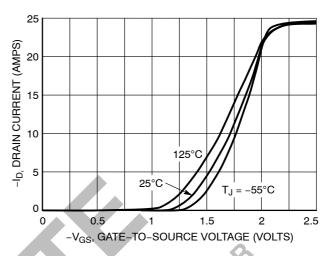


Figure 2. Transfer Characteristics

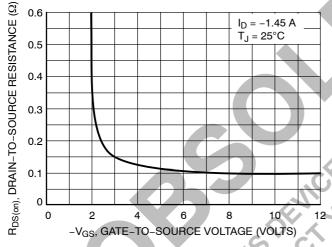


Figure 3. On-Resistance vs. Gate-to-Source Voltage

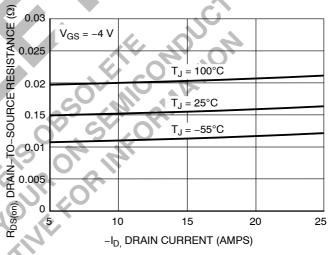


Figure 4. On–Resistance vs. Drain Current and Temperature

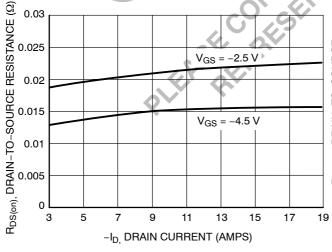


Figure 5. On-Resistance vs. Drain Current and Gate Voltage

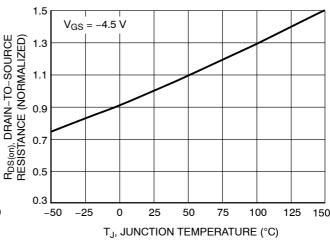
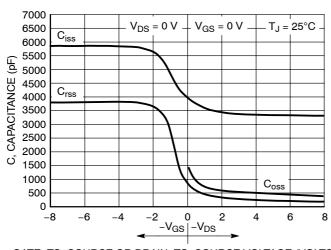


Figure 6. On–Resistance Variation with Temperature

# TYPICAL PERFORMANCE CURVES (T<sub>J</sub> = 25°C unless otherwise noted)



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 7. Capacitance Variation

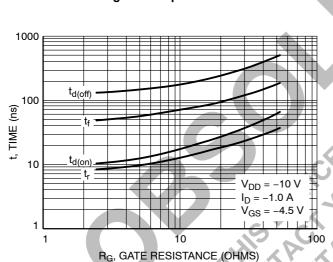


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

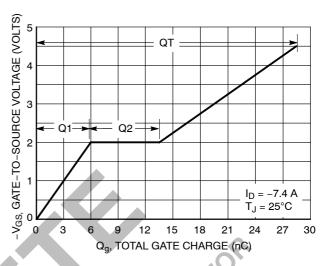


Figure 8. Gate-to-Source Voltage vs. Total Gate Charge

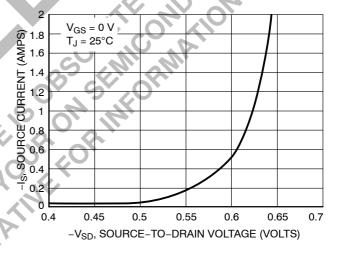


Figure 10. Diode Forward Voltage vs. Current

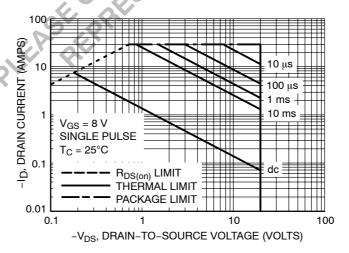
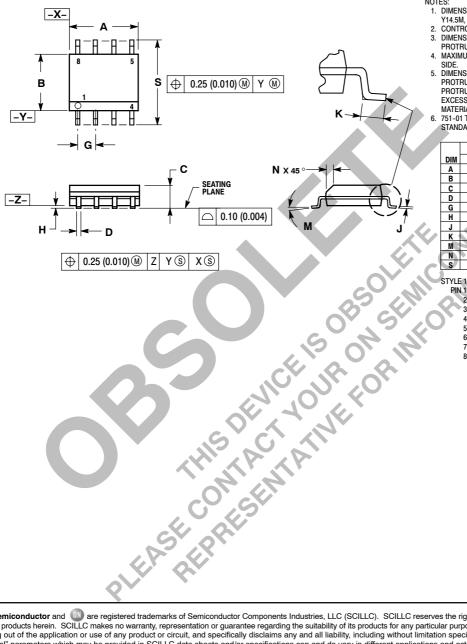


Figure 11. Maximum Rated Forward Biased Safe Operating Area

### NTMS4101P

### PACKAGE DIMENSIONS

## SOIC-8 NB CASE 751-07 **ISSUE AA**



#### NOTES

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 751-01 THRU 751-06 ARE OBSOLETE, NEW STANDARD IS 751-07.

	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	4.80	5.00	0.189	0.197	
В	3.80	4.00	0.150	0.157	
U	1.35	1.75	0.053	0.069	
D	0.33	0.51	0.013	0.020	
G	1.27 BSC		0.050 BSC		
H	0.10	0.25	0.004	0.010	
7	0.19	0.25	0.007	0.010	
K	0.40	1.27	0.016	0.050	
M	0	. 8°	0 °	8 °	
8	0.25	0.50	0.010	0.020	
g	5.80	6.20	0.228	0.244	

- SOURCE
  - SOURCE SOURCE
- GATE
- DRAIN DRAIN
- DRAIN

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